

FRANCESCO SPADINI

EDUCATION

Jan. 2001-Present University of Illinois Urbana, IL
Ph.D. in Electrical Engineering

- Overall GPA: 3.8
- Research Interests: Computer Architecture and Dynamic Reoptimization
- Expected Graduation Date: December 2006

1997-2000 University of Illinois Urbana, IL
Bachelor of Science in Computer Engineering

- Overall GPA: 3.63, Technical GPA: 3.58
- Eta Kappa Nu Member and Tutor

WORK EXPERIENCE

May-August 2002 Advanced Micro Devices Austin, TX
Computer Architecture/Performance Modeling

- Correlated execution-driven and trace-driven model performance
- Developed branch characterization tool to aid branch prediction research

May-August 2001 Advanced Micro Devices Austin, TX
Computer Architecture/Performance Modeling

- Developed execute logic for execution-driven timing model
- Interfaced timing model with full-system simulator

Spring 2000-Spring 2002 University of Illinois Urbana, IL
ECE 312 Teaching Assistant

- Lectured students on how to debug VHDL projects
- Wrote specifications for and managed final project
- Helped students with projects in laboratory setting

PUBLICATIONS

- F. Spadini, B. Fahs, S. J. Patel, and S. S. Lumetta. "Improving Quasi-Dynamic Schedules Through Region Slip," To Appear in the Proceedings of the First International Conference on Code Generation and Optimization, April 2003.
- F. Spadini, M. Fertig, and S. J. Patel. "Characterization of Repeating Dynamic Code Fragments," Center for Reliable and High-Performance Computing Technical Report CRHC-02-09.
- B. Slechta, D. Crowe, B. Fahs, M. Fertig, G. A. Muthler, J. Quek, F. Spadini, S. J. Patel, and S. S. Lumetta. "Dynamic Optimization of Micro-Operations," To Appear in the Proceedings of the 9th International Symposium on High-Performance Computer Architecture, February 2003.
- F. Spadini and G. A. Muthler. "Improving DLL Performance with Dynamic Optimizations," Proceedings of the First Annual Illinois Computer Systems Symposium, May 2002.
- B. Fahs, S. Bose, M. Crum, B. Slechta, F. Spadini, T. Tung, S. J. Patel, and S. Lumetta. "Performance Characterization of a Hardware Framework for Dynamic Optimization," Proceedings of the 34th International Symposium on Microarchitecture, December 2001.

COURSE PROJECTS

Andersen's Algorithm for Interprocedural Alias Analysis

- Implemented offline variable substitution and online cycle elimination
- Analyzed the impact of Andersen's algorithm in LLVM, a link-time optimizer

Survey of Dynamic Optimization Systems

- Analyzed correctness issues involved in software and hardware optimizers
- Case studies: Dynamo, DyC, DAISY, rePLay, ROAR, JUDO
- Won best project award

Performance of Store Buffer Implementations in the context of rePLay

- Implemented store buffer optimizations on the rePLay microarchitecture
- Analyzed their impact on average store buffer size and performance metrics

RELEVANT COURSEWORK

- ECE 325 - VLSI Design
- ECE 411 - High-Performance Computer Architectures
- ECE 412 - Advanced Computer Architecture
- ECE 433 - Multiprocessor Architectures
- CS 426 - Advanced Compiler Construction