

# *Curriculum Vitae – Sanjay J. Patel*

## **CONTACT INFORMATION**

262 Computer and Systems Research Laboratory  
University of Illinois at Urbana-Champaign  
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## **RESEARCH INTERESTS**

Processor Microarchitecture, Computer Architecture, Compiler Optimization, Error-Tolerant Computing, Memory Systems.

## **EDUCATION**

University of Michigan, Ann Arbor, BSE in Computer Engineering, 1990  
University of Michigan, Ann Arbor, MSE in Computer Science and Engineering, 1992  
University of Michigan, Ann Arbor, PhD in Computer Science and Engineering, 1999

## **HONORS AND AWARDS**

IBM Faculty Partnership Award, 2003-2004, 2004–2005  
University of Illinois Willett Faculty Scholar, 2002–2005  
Incomplete List of Instructors Ranked Outstanding by Their Students, UIUC, 2000–2003  
National Science Foundation, CAREER Award, 2001  
Intel Foundation, Intel Graduate Fellow, 1998–1999  
Amer. Society of Engineering Education, Outstanding Graduate Student Instructor, 1995–1996

## **EMPLOYMENT HISTORY**

Assistant Professor of Electrical and Computer Engineering, Research Assistant Professor in the Coordinated Science Laboratory, University of Illinois at Urbana-Champaign, Urbana, IL	Aug 1999–Present
Summer Associate, Intel Corporation, Portland, OR and Santa Clara, CA	May 1996-Aug 1996 May 1997-Aug 1997
Hardware Engineer, Digital Equipment Corporation, Hudson, MA	June 1992–August 1995

## **CONSULTING ACTIVITIES**

AGEIA Technologies, Feb 2004–present  
Intel Corporation, May 2002—Aug 2002  
Jet Propulsion Laboratory, Sept 2000–April 2002  
Transmeta Corporation, June 2000–Feb 2001  
HAL Computer Systems, Feb 1998–Aug 1998

## PUBLICATIONS

### Archival Journal Papers

Ronald D. Barnes, John W. Sias, Erik M. Nystrom, Sanjay J. Patel, Nacho Navarro and Wen-mei W. Hwu, "Beating in-order stalls with 'flea-flicker' two-pass pipelining", IEEE Transactions on Computers, Special Issue on Embedded Systems, Microarchitecture and Compilation Techniques, in Memory of B. Ramakrishna (Bob) Rau, Feb. 2006

S. J. Patel and S. S. Lumetta, "rePLay: A Microarchitectural Framework for Dynamic Program Optimization," IEEE Transactions on Computers, IEEE Transactions on Computers, February 2001.

S. J. Patel, D. H. Friendly, and Y. N. Patt, "Evaluation of Design Options in the Trace Cache Fetch Mechanism." IEEE Transactions on Computers, Special Issue on Caches and Related Problems, February 1999.

D. McKinney, M. Bhaiwala, K. A. Chui, C. Houghton, J. Mullens, D. Liebholz, S. J. Patel, D. Ramey, M. Rosenbluth, "The Design and Verification of a Low-Cost Alpha Microprocessor," Digital Technical Journal, Volume 6, Number 1, Winter 1994.

### Refereed Conference Papers

Nicholas Wang and Sanjay J. Patel, "ReStore: A Symptom-Based Processor Architecture for Soft-Error Tolerance", to appear 11<sup>th</sup> International Symposium on Dependable Systems and Networks, June 2005.

Brian Fahs, Todd Rafacz, Sanjay J. Patel, Steven S. Lumetta, "Continuous Optimization," to appear: 32<sup>nd</sup> Annual International Symposium on Computer Architecture, June 2005.

Nicholas Wang, Todd Rafacz, Justin Quek, and Sanjay J. Patel, "Characterizing the Effect of Transient Faults on a High-Performance Pipeline," 10<sup>th</sup> International Symposium on Dependable Systems and Networks, June 2004.

Todd Ehrhart and Sanjay J. Patel, "Reducing the Scheduling Critical Cycle using Wakeup Prediction," 10<sup>th</sup> Annual Symposium on High-Performance Computer Architecture, February 2004.

Ronald D. Barnes, Erik M. Nystrom, John W. Sias, Sanjay J. Patel, Nacho Navarro, Wen-mei W. Hwu, "Beating In-Order Stalls with "Flea-Flicker" Two-Pass Pipelining," 36<sup>th</sup> Annual International Symposium on Microarchitecture, December 2003.

Nicholas Wang, Michael Fertig, and Sanjay J. Patel, "Y-Branched: When You Come to a Fork in the Road, Take It," 12th International Conference on Parallel Architectures and Compilation Techniques, pages 56-67, Sept 2003.

S. S. Lumetta and S. J. Patel, "Characterization of Essential Dynamic Instructions", 2003 International Conference on Measurement and Modeling of Computer Systems, *ACM SIGMETRICS*, June 2003.

F. Spadini, B. Fahs, , S. J. Patel, S. S. Lumetta, "Improving Quasi-Dynamic Schedules using Region Slip", 1<sup>st</sup> Annual Symposium on Code Generation and Optimization, March 2003.

B. Slechta, B. Fahs, G. Muthler, J. Quek, F. Spadini, D. Crowe, M. Fertig, S. J. Patel, S. S. Lumetta, "Dynamic Optimization of Micro-instructions", 9<sup>th</sup> Annual Symposium on High-Performance Computer Architecture, February 2003.

G. Muthler, D. Crowe, S. J. Patel, S. S. Lumetta, "Instruction Deferral Using Static Slack", 35<sup>th</sup> Annual Symposium on Microarchitecture, November 2002.

B. Fahs, S. Bose, M. Crum, B. Slechta, F. Spadini, T. Tung, S. J. Patel, S. S. Lumetta, "Performance Characterization of a Microarchitectural Framework for Dynamic Optimization," 34<sup>th</sup> Annual Symposium on Microarchitecture, December 2001.

S. J. Patel, T. Tung, S. Bose, and M. Crum, "Increasing the Size of Atomic Instruction Blocks using Control Flow Assertions," 33<sup>rd</sup> Annual Symposium on Microarchitecture, December 2000.

D. H. Friendly, S. J. Patel, and Y. N. Patt, "Putting the Fill Unit to Work: Dynamic Trace Optimizations for Trace Cache Microprocessors," 31<sup>st</sup> Annual Symposium on Microarchitecture, December 1998.

S. J. Patel, M. Evers, and Y. N. Patt, "Improving Trace Cache Effectiveness with Branch Promotion and Trace Packing," 25<sup>th</sup> Annual International Symposium on Computer Architecture, July 1998.

M. Evers, S. J. Patel, and Y. N. Patt, "An Analysis of Correlation and Predictability: Why Two-Level Branch Predictors Work," 25<sup>th</sup> Annual International Symposium on Computer Architecture, July 1998.

D. H. Friendly, S. J. Patel, and Y. N. Patt, "Alternative Fetch and Issue Policies for the Trace Cache Fetch Mechanism," 30<sup>th</sup> Annual International Symposium on Microarchitecture, December 1997.

### **Magazine Articles**

Y. N. Patt, S. J. Patel, M. Evers, D. H. Friendly, and J. Stark, "One Billion Transistors, One Uniprocessor, One Chip," IEEE Computer, September 1997.

### **Textbooks**

Y. N. Patt and S. J. Patel, Introduction to Computing Systems : From Bits and Gates to C and Beyond, McGraw-Hill, Inc, Second Edition, August 2003.

## Technical Reports

F. Spadini, M. Fertig, S. J. Patel, S. S. Lumetta, "Characterization of Repeating Code Fragments," University of Illinois Technical Report, CRHC-02-09, October 2002.

S. J. Patel and S. S. Lumetta, "rePLay: A Framework for Dynamic Program Optimization," University of Illinois Technical Report, CRHC-99-16, December 1999.

S. J. Patel, D. H. Friendly, and Y. N. Patt, "Critical Issues Involving the Trace Cache Fetch Mechanism," University of Michigan Technical Report, CSE-TR-335-97, May 1997.

## Workshop Papers

S. J. Patel, W. Magda, Z. Kalbarczyk, and R. K. Iyer, "Processor-Level Framework for High-Performance and High-Dependability," Workshop on Evaluating and Architecting Systems for Dependability, June 2001

S. S. Lumetta, S. J. Patel, B. Fahs, and S. Bose, "Symbolic Verification of Dynamic Optimization in Microprocessors," In Supplement of the 2001 International Conference on Dependable Systems and Networks

J. Xu, Z. Kalbarczyk, R. K. Iyer, S. J. Patel, "Architectural Support for Stack Smashing Attacks," Workshop on Evaluating and Architecting System Reliability, Oct 2002.

F. Koopmans and S. J. Patel, "Decoupled Pipelines: Rational, Analysis, and Evaluation", Workshop on Globally Asynchronous, Locally Synchronous Designs, June 2002.

S. J. Patel, Z. Kalbarczyk, R. K. Iyer, W. Magda, N. Nakka, "A Processor-level Framework for High-Performance and High-Dependability," Workshop on Evaluating and Architecting System Reliability, June 2001.

S. S. Lumetta, S. J. Patel, S. Bose, B. Fahs, "The Symbolic Verification of a Hardware-based Dynamic Optimizer," Fast Abstracts, International Symposium on Dependable Systems and Networks, June 2001.

## GRADUATE STUDENTS ADVISED

### M.S. Thesis Students (16 total)

Satarupa Bose, MSE 2001	David Crowe, MSE 2004
Matthew Crum, MSE 2001	Brian Fahs, MSE 2002
Michael Fertig, MSE 2003	Jeff Hassan, MSE 2003
John Liao, MSE 2002	Wojciech Magda, MSE 2002
Aqeel Mahesri, MSE 2004	Ali Mushtaq, MSE 2002
Jeffrey Namkung, MSE 2001	Justin Quek, MSE 2004
Brian Slechta, MSE 2003	Tony Tung, MSE 2001
Nicholas Wang, MSE 2003	Ashley Wise, MSE 2003

### Ph.D. Students (9 total, all anticipated graduations)

David Crowe, 2006	Todd Ehrhart, 2006
Brian Fahs, 2005	Aqeel Mahesri, 2006
Gregory Muthler, 2006	Justin Quek, 2007
Galen Rasche, 2007	Francesco Spadini, 2006
Nicholas Wang, 2005	

## MAJOR FUNDING SOURCES

2001-2006	National Science Foundation CAREER Award	approx \$300,000
2001-2002	MARCO/Center for Circuits, Systems, and Software	approx \$100,000
2003-2006	MARCO/Center for Circuits and Systems Solutions	approx \$375,000
2001-2005	Intel Research Gifts (equipment and money)	approx \$130,000
2000-2004	AMD Research Gifts (equipment and money)	approx \$ 30,000
2002-2005	Sun Research Gifts (equipment and money)	approx \$ 90,000
2003-2005	IBM Research Gifts (money)	approx \$ 60,000
2004-2007	National Science Foundation CPA Grant (3 PIs)	approx \$ 50,000
2004-2007	National Science Foundation CPA Grant (2 PIs)	approx \$400,000