Logic Soft Errors in Servers

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Abstract

It has been known for a significant period of time that radiation has a negative impact on reliability of integrated circuits. In late seventies several landmark papers pointed out that single event upsets (SEU) were induced in semiconductor memories by the cosmic ray flux [1,9] and radioactive contamination [4]. Since then extensive research was conducted for studying this phenomenon and finding solutions for lowering circuit sensitivity to particle induced errors [2, 6, 10, 11].

Today, the impact of SEU on computing systems is even more significant due to the aggressive scaling of the semiconductor manufacturing processes. The increased soft error rates (SER) experienced by the logic circuitry has also become a concern [3, 7]. Last but not least, the higher integration and complexity of VLSI circuits, in general, and microprocessors in particular, has been leading to a continuously higher device count per unit of chip area. As a result, SER estimation and measurement have become essential for ensuring adequate reliability.

This work concentrates on estimating the impact of logic soft errors on a computing system. First, the trends of logic SER are discussed. Saturation and even a slight decrease of the logic SER per bit is observed, as semiconductor manufacturing evolves. Notably, the logic SER at the chip level is increasing by almost one order of magnitude, over four generations of silicon manufacturing processes, due to the higher integration.

Second, SER estimation methodology is discussed. Primarily, our approach is based on deriving the nominal rate of a circuit and the timing (TD) and logic (LD) derating factors. TD is the fraction of time the circuit is susceptible to SEU, while LD is the probability that SEU impacts the behavior of the system. Both simulated fault injection and accelerated neutron testing showed that a

significant fraction of the soft errors actually vanish without causing any system misbehavior. As a result, the SER of a circuit element is given by the following equation [5]:

Element SER = Nominal SER * TD * LD

Furthermore, a complex integrated circuit, processor or chip-set, for instance, consist of two main entities, machine states (MS) and non-machine states (non-MS). MS are critical to the normal operation, as they represent the state of the machine at any moment in time. Examples are application and control registers and memory structures, like caches and translation look-aside buffers [5]. TD and LD take different values, for MS and non-MS, as it will be shown later.

In the case of MS latches the stored state is vulnerable to SEU at all times and, as a result, TD is one. For sequentials designated as non-MS, TD depends on the type of sequential, as well as on the logic path length of each stage in the data or control path. Recent studies [8] have shown that the TD decreases as a function of propagation delay introduced by the combinational logic located in the paths between the sequentials. The reason is that for an upset induced in one of the sequential nodes to be of relevance, it has to propagate to the next downstream sequential and arrive there at least a setup time before the clock asserts. If the corrupted data arrives too late it will not be latched and will not cause an error. For flow-through and m/s FF based designs, the TD varies between 0.5 for the shortest paths and about 0 for critical paths, i.e. for critical paths the SER contribution of a sequential becomes negligible.

The calculation of the average TD factor for sequentials located in a block or on a chip involves two steps:

1. Modeling the dependence of TDs on the propagation delay in the combinational logic at use conditions (i.e., for given Vcc, temperature, clock speed, etc) and
2. Extracting the distribution of propagation delays of paths located in the fub or chip under investigation.

The average TD of a circuit block can then be estimated by integrating the sequential TD over the corresponding delay distributions (one for flip flops, one for latches, etc). Using min delay statistics for the delay distribution to bound the average TD conservatively, we typically observe TD values of the order of 30% or less for modern high speed microprocessors. The same strategy can be applied to determining TD factors of other types of sequentials as well as dynamic logic.

TD of the combinational logic is different for the data path and control logic. In the case of static data path a particle induced glitch may be stored if it reaches a latch within the set-up time (S) –

hold time (H) window. As a result the following equation can be used for calculating TD of a single gate [5]:

$$TD = (S+H+W)/T$$

where W is the width of the glitch generated by the particle strike and T is the clock period. Glitches in the control path may cause false writes into storage cells, e.g. write into a latch which is in store mode. More details on time derating, including the case of dynamic logic are available in [5].

Logic derating takes into consideration the utilization of different resources available in a complex integrated circuit, like a processor or chip-set. For instance, if an I/O buffer contains valid data 40% of the time, the LD is 0.6. In other words, 60% of the particle strikes will have no impact on the operation of the machine, as they modify stale data. Similarly, LD is 0.5, if 64-bit words are written into a 128-bit wide buffer. Performance simulators can be used for deriving LD of different functional blocks, both in the case of MS and non-MS. However, it has to be stressed that some MS, like configuration registers, contain valid information all the time and, as a consequence, cannot be derated, i.e. LD = 1.

Next, we evaluate the impact of soft errors on a typical microprocessor and a chip-set. Errors experienced by latches, combinational logic, SRAM and I/O circuitry are considered. The SER effect is evaluated without and with parity/ECC protection of the SRAM arrays. The analysis shows that functional blocks employing large numbers of latches/flip-flops and combinational logic, experience high SER.

Lastly, we asses the impact of logic SER on a generic server. Assuming that the main storage arrays, such as cashes and large buffers, employ data integrity protection, the main contributors to the system SER are latches and combinational logic.

Serious challenges face our attempts of assessing the impact of SER logic at the system level. Estimation of the nominal rates and derating factors, early in the development process, is required for the effective mitigation of high SER. The accurate computation of the TD and LD, in the case of complex circuits, requires additional research and the automation of SER evaluation needs significant improvement. Although technical solutions are available for mitigating the impact of increasing SER, cost effectiveness is a difficult to achieve desiderate.

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